

## CLAIMS

1. A method for manufacturing an integrated circuit comprising a nonvolatile memory, the method comprising:

5 forming a first structure over a semiconductor substrate, the first structure comprising:

a first conductive gate of a nonvolatile memory cell; and

a first dielectric over the first conductive gate;

10 forming a layer ("FG layer") to provide at least two conductive floating gates for the memory cell, wherein each floating gate comprises a first portion and an upward protruding second portion, the second portion being formed over the first dielectric and overlaying a sidewall of the first conductive gate.

2. The method of Claim 1 wherein the FG layer comprises a first sub-layer and a second sub-layer formed after the first sub-layer, wherein the first portion of each floating gate is formed from the first sub-layer, and the second portion of each floating  
15 gate is formed from the second sub-layer.

3. The method of Claim 2 wherein forming the FG layer comprises:

forming the first sub-layer to provide the first portions of the floating gates, the first structure protruding above the first sub-layer; and then

20 forming the second sub-layer layer and etching the second sub-layer to provide the second portions of the floating gates on sidewalls of the first structure.

4. The method of Claim 1 wherein the FG layer consists of one or more sub-layers all of which are present in both the first and the second portions of the floating  
25 gates.

5. The method of Claim 4 wherein forming the FG layer comprises:

forming the FG layer over the first structure; and then

etching the FG layer anisotropically without a mask over the memory cell to remove the FG layer from over the top of the first structure but leave the FG layer over the first dielectric over the sidewall of the first structure.

- 5        6.        The method of Claim 5 further comprising forming substrate isolation regions, each substrate isolation region being a dielectric region having a portion protruding above the semiconductor substrate;

wherein forming the FG layer over the first structure results in the FG layer having a greater thickness between the substrate isolation regions next to the first structure than over the substrate isolation regions;

- 10        wherein etching the FG layer results in the FG layer being etched off from over at least portions of the substrate isolation regions and the first structure but not between the substrate isolation regions next to the first structure.

- 15        7.        The method of Claim 1 wherein the memory cell is one of a plurality of the memory cells, and the method further comprises a masked etch of the FG layer to remove portions of the FG layer between different memory cells.

8.        The method of Claim 1 further comprising forming two second conductive gates for the memory cell, the second conductive gates being insulated from the first conductive gate and the floating gates.

- 20        9.        The method of Claim 8 wherein forming the FG layer to provide the floating gates comprises:

forming the FG layer;

forming a dielectric D1 over the FG layer;

- 25        forming a layer G2 over the dielectric D1, wherein each second conductive gate comprises a portion of the layer G2, wherein the layer G2 has a portion P1 protruding above the first conductive gate;

forming a layer L1 over the layer G2 such that the protruding portion P1 is exposed and not completely covered by the layer L1;

at least partially removing the protruding portion P1 to form a through hole in the layer G2 over the first conductive gate, wherein at a conclusion of this removing operation a portion of the layer G2 remains covered by the layer L1;

forming a layer L2 on the layer G2 adjacent to the through hole; and

5 removing at least parts of the layers L1 and G2 and of the FG layer selectively to the layer L2.

10. An integrated circuit comprising:

a semiconductor substrate;

a first dielectric region on the semiconductor substrate;

10 a first conductive gate of a nonvolatile memory cell on the first dielectric region;

two second dielectric regions of the memory cell on the semiconductor substrate;

two conductive floating gates of the memory cell on the respective second dielectric regions, each floating gate comprising a first portion and an upward protruding second portion.

15 11. The integrated circuit of Claim 10, wherein in any horizontal cross section by a plane passing through the upward protruding second portions and the first conductive gate, the distance between each of the upward protruding second portions and the first conductive gate is smaller than the width of the first conductive gate.

20 12. The integrated circuit of Claim 10 wherein in top view the distance between each of the upward protruding portions and the first conductive gate is smaller than the width of the first conductive gate.

13. The integrated circuit of Claim 10 wherein the memory cell further comprises two second conductive gates overlying at least portions of the respective two floating gates but not overlying the first conductive gate;

25 a dielectric insulating the floating gates from the first and second conductive gates, and insulating the first conductive gate from the second conductive gates.

14. The integrated circuit of Claim 13 wherein an overlap between each of the upward protruding portions and the respective second conductive gate is at least as large as the thickness of each the second conductive gates.

15. The integrated circuit of Claim 13 wherein an overlap between each of the upward protruding portions and the respective second conductive gate is at least 0.08 $\mu$ m.

16. The integrated circuit of Claim 13 wherein the top of each second conductive gate is not higher than the top the respective upward protruding portion.

17. The integrated circuit of Claim 13 wherein the top of each second conductive gate is lower than the top of the respective upward protruding portion.

18. The integrated circuit of Claim 13 wherein each upward protruding second portion of the floating gate is between the respective second conductive gate and the first conductive gate.

19. The integrated circuit of Claim 10 further comprising a dielectric over sidewalls of the first conductive gate, wherein each upward protruding second portion is formed as a spacer on the dielectric over the respective sidewall of the first conductive gate.